13. (currently amended) A The digital circuit design verification tool in accordance with claim 12, further comprising an arranging unit, coupled to said minimum width determination unit, to arrange coarse granularities in terms of an equivalence class structure with an initial satisfiability problem considered as a number of independent satisfiability problems.

REMARKS

The Abstract and the Specification were objected to.

Claims 1, 2, and 9 were objected to.

Claim 8 and 9-13 were rejected under 35 U.S.C. §112, first paragraph.

Claims 2 and 9 were rejected under 35 U.S.C. §112, second paragraph.

Claims 1-2 and 8-9 were rejected under 35 U.S.C. §102(b) as being anticipated by Dangelo et al (USPN 5,598,344).

Claims 3-7 and 10-13 would be allowed if suitably rewritten.

In accordance with the foregoing, the specification and claims 1-13 have been amended. No new matter has been added.

Claims 1-13 are pending and under consideration.

ABSTRACT:

The Abstract has been amended and is now believed to be in allowable form.

SPECIFICATION:

The specification has been amended to clarify the meaning of N_+, although the meaning is believed to be clear to those skilled in the art.

CLAIM OBJECTIONS:

Claims 1, 2 and 9 have been amended and are now believed to be clear.

REJECTION UNDER 35 U.S.C. §112:

Claim 8 has been amended to recite two elements; thus, the objections to claim 9 and claims 9-13 depending therefrom are now believed to be moot.

Claims 2 and 9 have been amended to define the meaning of N_+, although the meaning is believed to be clear to those skilled in the art.

REJECTION UNDER 35 U.S.C. §102:

In the Office Action at pages 2-4, the Examiner rejected claims 1-2 and 8-9 under 35 U.S.C. §102(b) as being anticipated by Dangelo et al. (USPN 5,598,344; hereafter referenced as Dangelo et al.).

The rejection is respectfully traversed and reconsideration is requested.

It is respectfully submitted that the field of technology of the present invention is different from that of Dangelo et al. That is, the present invention relates to formal verification of electronic circuits. In general, the present invention relates to a method and an apparatus to obtain an RTL model suitable for formal verification. RTL models conventionally used for formal verification use signals of comparatively high signal width. Thus, using such RTL specifications for formal verification is quite time consuming.

Hence, the present invention was developed to provide an RTL specification that is better suitable for formal verification.

In accordance with embodiments of the present invention, the conventional RTL specification is processed to obtain a reduced RTL specification, i.e., an RTL specification wherein the width of the signals is reduced. See examples on pages 8-10 of the present specification.

In contrast, Dangelo et al. teaches to a method to obtain an RTL description from a higher level (e.g., VHDL) description (see column 2, lines 56-60 of Dangelo et al.) Thus, the method disclosed by Dangelo et al. may be used before the method of the present invention to obtain a RTL specification of the circuit in question, and then the method of the present invention may be used to obtain a reduced RTL specification.

In the outstanding Office Action, the Examiner refers to the techniques for scaling disclosed in Dangelo et al. and states that scaling also includes a reduction of the RTL model. This is in contrast to the specification of Dangelo et al., wherein in col. 53, lines 21-23, it is

explicitly states that "these module replication strategies can be employed to accomplish virtually any type of (upward) scaling of a model design." It is respectfully submitted that this means that a reduction of signal width, as is accomplished by the present invention, which may be interpreted as a form of downward scaling, is explicitly excluded.

It is inherent to the method disclosed in Dangelo et al. that downward scaling is not possible, since the scaling relies on replicating modules (see column 51, lines 64-67). Replicating or duplicating modules cannot result in downward scaling.

The references to a width n (column 32, line 60 or column 35, line 5 of Dangelo et al.) relate in both cases only to general design consideration for the circuit in question as regard for example, I/O buses. Thus, it is respectfully submitted that these references are in no way connected with a reduction of a width of a signal to obtain a reduced RTL model.

Hence, since Dangelo et al. does not relate to obtaining a reduced RTL model from an existing RTL model, it is respectfully submitted that Dangelo et al. does not teach or suggest the subject matter of the present invention and does not anticipate claims 1-2 and 8-9 under 35 U.S.C. §102(b).

ALLOWABLE CLAIMS:

Applicant respectfully submits that independent claims 1 and 8 have been amended and are now in form for allowance. Thus, the claims depending therefrom, claims 2-7 and 9-13, respectively, are also allowable for at least the reasons that amended claims 1 and 8 are allowable.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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Date: July 14 2003

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